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Optimized Design of ALU for Low Power Dissipation

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Abstract-Power dissipation has a major impact while we are designing any circuit. Since this factor plays a major role in deciding the efficiency of the designed circuit i.e. why in this paper we are proposing a plan for sequential circuits so that we can reduce the power dissipation. power dissipation which in turn reduces the whole power dissipation of CPU [1]. With this we can reduce the overall power dissipation substantially in the circuit. In this paper the comparative analysis of various comparator circuit design of ALU is presented to reduce Power dissipation of CPU [1]. Three Comparator circuits chosen for comparison are: Traditional comparator, Domino Style comparator and Pass Logic Based Single Stage Comparator.

Keywords- Tanner tools, Comparator,ALU,power Dissipation

I. INTRODUCTION

Power dissipation is basically the power which is converted to heat and then conducted or radiated away from the device. Electronic and electric devices can have a limit on the current they can safely handle that is not an electronic limit, but a physical one. For instance, a transistor may otherwise be able to handle a certain amount of current, but it is given a lower current rating because the die gets too hot. Dissipation is usually measured in watts, and uses the usual Ohm's law calculations for power.

Eficiency ∞ 1/power dissipation

In this paper, we introduce two fast CMOS comparators, capable of comparing up to 8 bits that dissipate energy predominantly on a full or a partial match in the bit positions of the comparands.

II. PROPOSED IDEA FOR LOW POWER DISSIPATION IN ALU

Power dissipation in CPU can be reduced in case we consider the complete internal architecture of CPU and then reduce its power dissipation in different parts. As we can easily analyze that CPU have two main units: CU (Control Unit) and ALU (Arithmetic and logic unit).In case we are able to reduce power dissipation in any of the above two we can reduce the overall power dissipation for CPU. In this paper we consider ALU as our device in which we will reduce the power dissipation and hence the overall power dissipation for CPU will be reduced

III. ALU (ARITHMETIC AND LOGIC UNIT)

ALU is the most important part of CPU which can be used as a tool to reduce the power dissipation in device. The figure given below shows the internal architecture of ALU. In ALU as we know we have four blocks. The Add/Sub block[2], Comparator block, Logical unit block and Shift/rotate block. The four blocks performs the functions as required. For example, if we want to perform comparison operation then it is performed with the help of Comparator block.

The comparator block performs equal, not equal and signed or unsigned, greater or equal and less than comparisons .

To get all these tasks accomplished we have to design a circuit which can perform the functioning given in above table. We can implement this with three styles:

operation	opcode	Logical function
A≥B	001	$(\overrightarrow{A_{31}.B31})+diff_{31}.(\overrightarrow{A_{31}} \oplus \overrightarrow{B_{31}})$
$A < B$	010	$(A_{31} \overrightarrow{B_{31}}) + dif_{31} (\overrightarrow{A_{31}} \oplus B_{31})$
A=B	011	$\overrightarrow{ZERO}$
A=B	100	ZERO
$A \geq B$	101	CARRY
A<B	110	$\overrightarrow{CARRY}$

Table1: Operation of comparator

IV.A TWO-STAGE DOMINO-STYLE COMPARATOR

represents a noticeable improvement, mainly in terms of response time, over our earlier proposed design based on three stages of domino logic.

The circuit of Figure 2 compares two 8-bit comparands, A7A6..A0 and B7B6..B0 using a combination of domino-style logic and pass transistor logic. P-transistor pass logic blocks (such as P in Figure 2) compare two bits of the comparands at a time. A high voltage level V_S is passed on to the right by each of these P-transistor blocks when both input bits that they compare match. Each P-transistor block drives the gate of an n-transistor (such as Q1) that is part of a discharge path of the domino logic stages. The precharging signal is cut off during the evaluation phase and an evaluation signal is applied to each stage of the domino logic. The first domino stage pulls down the output of the first stage during the evaluation phase only if the pass transistor logic using p-devices (greyed box, P) driving the gates of Q1 and Q2 are both on. This happens when all 4 least significant bits are equal. The n-transistors Q3 and Q4 prevent false matches caused by the charge accumulations in previous cycles. During precharging, these transistors turn on (dis is high) for a small time to discharge the charge stored in the previous cycle (which happens when the corresponding block matches) on the gates of transistors Q1 and Q2. The output of the comparator is discharged to

ground only when *all* bits of the comparands match.
To reduce the charge stored at the gates of transistors Q1, Q2, Q8 and Q9 and hence, the energy dissipated when these gates are discharged, a voltage lower than V_{dd} can be used as V_S. On the flip side, this increases the circuit delay on a match and complicates the design because the additional voltage source has to be provided (which can be either derived fromthe design because the additional voltage source has to be provided (which can be either derived from the outside of the chip or generated locally from the Vdd).

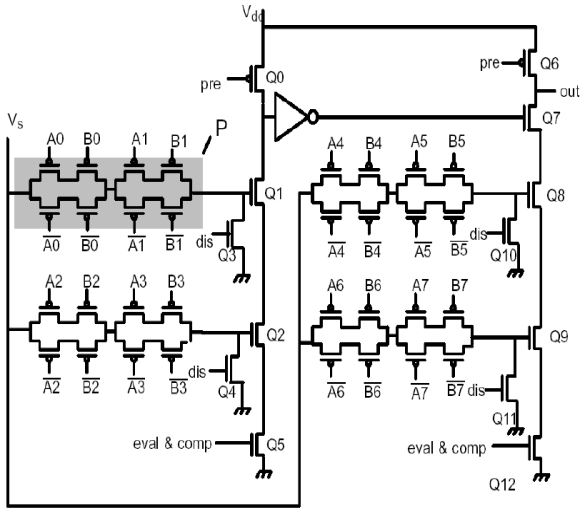

Fig1:Circuit Diagram of the Traditional Comparator

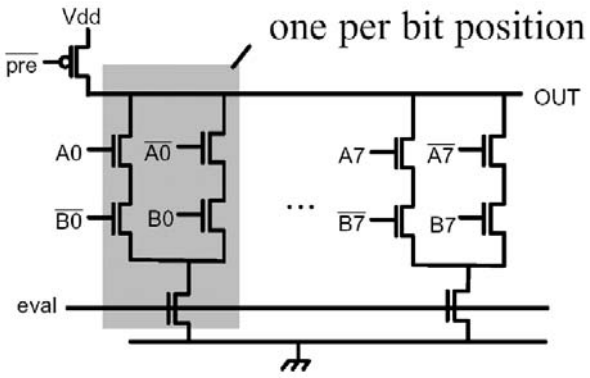

Fig2: Circuit Diagram of the 2-Stage Domino Comparator

The circuit shown in Fig. 2 compares two 8 bit comparands using a combination of domino- style logic and pass transistor logic. P-transistor pass logic blocks compare two bits of the comparands at a time. A high voltage is passed on to the right of each transistor block. The precharging signal is cut off during the evaluation phase and an evaluation signal is applied to each stage of the domino logic. The first domino stage pulls down the output of the first stage during the evaluation phase only if the pass transistor logic using p devices (greyed box, P) driving the gates of Q1 and Q2 are both on. This happens when all 4 least significant bits are equal. The n-transistors Q3 and Q4 prevent false matches caused by the charge accumulations in previous cycles. During precharging [6], these transistors turn on (this is high) for a small time to discharge the charge stored in the previous cycle (which happens when the corresponding block matches) on the gates of transistors Q1 and Q2. The output of the comparator is discharged to ground only when all bits of the comparands match. To reduce the charge stored at the gates of transistors Q1, Q2, Q8 and Q9 and hence, the energy dissipated when these gates are discharged, a voltage lower than Vdd can be used as Vs. On the flip side, this increases the circuit delay on a match and complicates the design because the additional voltage source has to be provided (which can be either derived On the flip side, this increases the circuit delay on a match and complicates

V.A PASS LOGIC, SINGLE STAGE COMPARATOR

The second proposed comparator design, shown in Figure3, avoids the use of domino-style logic altogether. The pass transistor logic shown within the greyed box in Figure 3 passes a high logic level to the gate of the n-transistor Q1 when bits A7 and B7, as well as bits A6 and B6 of the comparands match. The series pulldown structure consisting of the devices Q1, Q2, Q3 and Q4 thus conducts when all 8 bits of the comparands are equal. The output of this comparator, precharged to Vdd by Q0 is thus discharged when all bits of the comparands are equal and when the evaluate device, Q5, is on. The n-transistors Q6, Q7, Q8 and Q9 discharge any accumulated charges when partial matches occur, just as in the design of Figure 2. The effective loading of the output is small: the diffusion capacitances of a small p transistor (Q0) and an n-transistor (Q1), plus the gate capacitances of whatever is driven by the output and wire

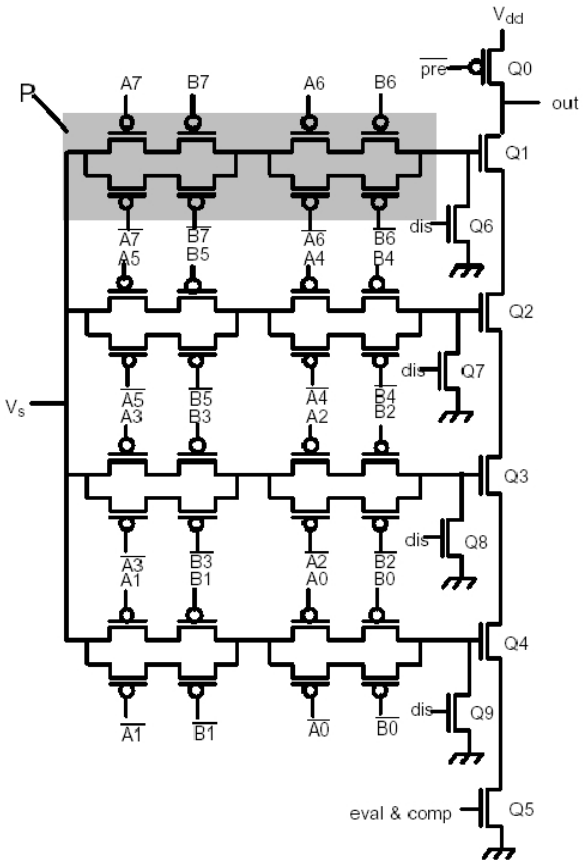

Fig3.Circuit Diagram of the Pass Logic Single Stage Comparator

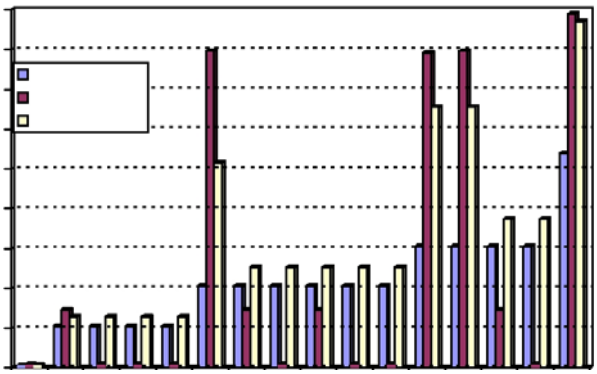

Fig4.Comparison of Dissipate-On-Match Comparators

VI. CONCLUSION

Traditional comparators used in several datapath artifacts of a modern processor are notoriously energy-inefficient as they dissipate energy on a mismatch in one or more bit positions. In scenarios, where matches occur relatively rarely, alternative comparator designs that dissipate energy predominantly on a full match are better alternatives.

VII. FUTURE WORK

As we have seen that power dissipation plays an important role in the functioning of every device. So it is required to minimize it. Hence we have to adapt certain strategies in order to reduce the power dissipation. In this report we have used the strategy of differential clocking i.e. if parts of a device are made to work on either positive edge triggering or negative edge triggering then only half the circuit works at a given time and hence half of the circuit is inactive. So the power dissipation factor reduces to half .

Hence we conclude that power dissipation is an important factor in determining the overall efficiency of circuits and by appropriately choosing the circuit and clocking strategy we can minimize the problems associated with power dissipation.

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